General Purpose Data Converters: Adaptability, Configurability, Scaling

Franco Maloberti

Department of Electronics, University of Pavia, Via Ferrata, 1 - 27100 Pavia - ITALY
E-mail: franco.maloberti@unipv.it

I. Abstract

Data converters used to interface the real-world with digital processors entail such a diverse requests that often using a case-by-case architecture and schematic is necessary. By constrat, modern digital systems are very flexible: just by changing software or programming the interconnections of digital arrays implements diverse standards and enables a great variety of processing functions. Result is that the analog interface is the bottleneck of general-purpose analog-digital processing systems. The solution frequently used is a multi-chip implementation which combines custom analog interfaces and general purpose microprocessors or field programmable gate arrays (FPGAs). An alternative method, discussed here, is to embed into digital VLSI chips a general purpose data converter with adaptable, re-configurable and scalable features, so as to provide a wide range of interfacing functions while consuming a proper level of power.

The key design parameters featuring data converters are resolution (the SNR), sampling frequency (or, better, signal band), linearity and power consumption. The first three parameters critically affecting power. In addition, depending on application, the conversion must provide a sample-by-sample conversion (as a Nyquist-rate architectures does) or ensure a suitable SNR and its equivalent number of bits (like oversampled data converters provide).

As know, defined specifications identify the optimal converter architecture and, actually, the first step of any data converter design is selecting algorithm and architecture. On the contrary a general purpose ADC must refer to a flexible algorithm and architecture so that by software reconfiguration it is possible to meet the widest range of requests. This require identifying algorithms, possibly hybrid, architectures and circuit schemes adaptable enough and configurable. Moreover, scaling the clock frequency and changing bias conditions can match speed and consumed power.

The optimal operational region of various algorithms in the sampling frequency-resolution plane is the starting point of this study. The architectures implementing various algorithms disclose possible configurability, the power-performance relationships direct power driven designs. We will see how analysis of algorithms and schemes indicates possibility to widen the region of operation while using the same schematic. The goal is identifying a general purpose data-converter.

Obtaining a wider range of frequency and resolution often involves digital control and extra processing in the digital domain but the corresponding cost is not a real issue because digital is cheap both in terms of silicon area and consumed power. In reality, it is not possible to have a universal scheme, but just solutions with enlarged region of use. They, in turn, significantly extend the number of applications with analog and digital processing needs that can be satisfied by a single-chip processor or FPGA.

After reviewing relevant conversion algorithms and circuit schemes this presentation discusses three possible general purpose architectures. The first is a Sigma-Delta/Incremental n-th order architecture ($n \leqslant 4$). The sampled-data operation enables an easy setting of the order and the number of bit of the quantizer. The use of a reset across the integrators changes the algorithm from $\Sigma\Delta$ to incremental. The correction of mismatch between elements is corrected with a DEM algorithm for $\Sigma\Delta$, or Smart DEM for incremental. The signal band and the oversampling determine the operation rate and, accordingly, the bias current of the op-amps.

A second example of general purpose ADC is two step architecture with SAR converters. The scheme can achieve 10-bit with more than 100 MS/s but can be configured to a 12-bit low speed scheme made by a plain SAR. The resolution can increase to 14-bit by an hybrid algorithmic-SAR configuration. The band of the input signal can go from low frequency (few kHz) to more than 50 MHz. The power consumption at low band is very low and goes to few mW for multi MHz band.

A third example is a digitally programmable pipeline/flash. The scheme enables selecting the number of stages and the bit determined in each stage. The scheme allows hundred of MS/s with low resolution ($\leqslant 6$ bit) and 10-12-bit for lower speeds. Power is not an optimal parameter.

In summary, the use of digital capabilities enables flexible data converter architectures adaptable to diverse requests, thus avoiding the bottleneck of analog interfaces in system integrated in a single chip.